Performance Analysis of Triangular Gate-all around Nanowire FETs with Si and GaAs as Channel Materials for Different Temperature values

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Abstract: In this paper, Triangular GAA NW FET has been designed for silicon and GaAs as channel materials of 20nm gate length. The performance of GAA NW FETs are calculated and compared in terms of transfer characteristics, output characteristics, I_{ON} current, switching speed, leakage current, Drain Induced Barrier Lowering (DIBL), Sub-threshold Swing (SS) and threshold voltage (V_{TH}). After comparison it was observed that GaAs NW FET is showing better performance i.e. low DIBL and low SS and lower leakage current where Silicon NW FET offers high on current. Further effects of temperature on the performance of the devices have been investigated with assist of 3D TCAD simulations. Investigation shows that GaAs NW FET shows better performance as compared to silicon NW FET in terms of leakage current, I_{ON}/I_{OFF} ratio and SCEs like SS and DIBL whereas Si NW FET show high on current (I_{ON}).

Keywords: GAA NW FET; TCAD; DIBL; SS; V_{TH}.

Introduction

In order to attain a novel device structure for the future CMOS technology, device engineer continuously scale down the channel length, oxide thickness and supply voltage in the past few decades. The downscaling of the above parameters of the transistor has results the remarkable improvement in the transistor potential, its size and cost. Actually the downscaling of transistor directly associated to increased speed, increased packing volume and low power dissipation [1].

Several unacceptable effects categorized as short channel effects are raised as the transistor is downscaled to nanometer domain. These effects can be lessened by enhancing the control of gate over the channel section and this will be attained in several ways such as, by reducing the thickness of oxide, by use of high dielectric materials, or by varying the device structure [2]. In 1984 the design of dual gate (DG) MOSFET was suggested by Hayashi and Sekigawa. This design became the first innovative structure which has ability to settle down the raised short channel effects. A new parameter, named electrostatic integrity (EI) presented by Skotinki describes gate controllability and applies to various types of MOSFETs. With the help of EI it is viable to estimate the rise in the subthreshold slope, V_{TH} roll off and drain induced barrier lowering. The worth of transistor is explained by the above three parameters and from these parameters is feasible to estimate the least possible gate length capable to offer good characteristics in off state. [3], [4].

MOSFETs with surrounding-gate [5] provide the best promising control over the channel and provides a very good characteristics in the subthreshold region and because of such characteristics, different firms are working on the production of nanowires with different channel materials and cross section from which we can discuss one of the most common structure having triangular cross section [6].

In this paper we focused on the GAA NWTs with triangular cross section. Electrical properties of GAA NWT having GaAs and silicon as channel material are investigated and compared. In particular, we discussed the influence of temperature on the device performance. Second part of the paper explains the GAA NW FET with silicon and GaAs as channel materials. Third part defines the device design for GAA NW FET with GaAs and silicon as channel material. Device simulation steps and performance are presented in next part and conclusion is given in last part.

GAA NW FET

Further down scaling in the nanometer regime, GAA NW FETs are the future candidates for the progress in CMOS scaling. GAA NW FETs can be produced in heavy quantity with repeated and reproducible electronics properties as essential for CMOS technology. Also, the channel diameter can be made less than 10nm without harming its electric characteristics. In addition, the charge scattering can be suppressed due to smoothening of surface, crystalline nature and the ability of radial

and axial NW hetro-structures. As the device dimensions are in nanometers, this leads to a very less mean free path which raise electrons drift velocity in the channel region and results an increment in the mobility.

Si NW FETs

Si NW FETs are receiving extra attraction because of their superior electrostatic integrity, superb conductive behavior, higher mobility and a very less scattering even at nanometer scale. Several kind of Si NW FETs are developed as a favorable candidate for the upcoming CMOS technology. In Si NW FETs silicon is used as a channel material. Like a planar MOSFETs, Si NWTs have metal source and drain terminals. Semiconductor-metal have exhibited positive schottky barriers which is a reasons of cumulative effects of work function of metal and fermi level pinning by various surface state. Thus significant effects on the device characteristics are shown by the properties of the contacts. Ohmic contacts are created by process of annealing, gradually raise the drive current and the mobility. During charge transportation within the structure carrier scattering is very less due to less mean free path of electrons with respect to device length [7].

GaAs NW FETs

GaAs NW FETs are more superior to Si NW FETs because of numerous advantages over Si NW FETs. GaAs semiconductor has higher electron mobility, which makes it more suitable for larger current (hence amplification). Due to higher electron mobility GaAs NWTs can be operated at much higher frequency as compared to silicon. GaAs semiconductor can be used for higher gain amplifier due to its very low noise characteristics and also one can amplify it to a greater extent without worrying about noise amplification. GaAs is a direct bandgap semiconductor which lends itself perfectly to LEDs [8].

Device Design

In this proposed work, GaAs and Si based GAA NWTs are designed with triangular cross section area. Fig. 1 shows a 1 Bird's eye view of GAA NW FET with triangular Fin.

Table 1. Architecture Parameters of Device

Architecture Parameter	Value (nanometer)
Lambda Design Rule	10nm
Structure orientation	<100>
Channel Height	10nm
Channel Diameter	10nm
Gate oxide	1nm
Channel length	20nm
Substrate Doping concentration	2e17
Source/drain (Doping concentration)	2.063e20
Channel Doping concentration	1e15

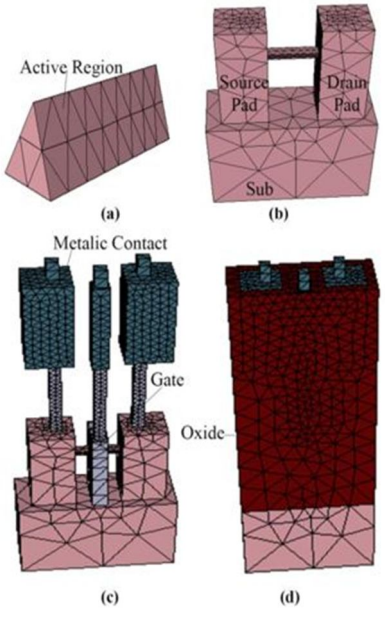

Fig.1 Bird's eye view of GAA NW FET with triangular fin illustrations; (a) Triangular shaped active region, (b) Active region with drain and source pad, (c) Formation of metallic gate and power supply contacts and (d) Formation of SiO_2 to separate each layer

In this work, Tungsten (W) (4.5eV) is used for gate terminal, gate oxide SiO_2 (k =3.9) is used to isolate the channel from gate, Source drain are made by W. Two different channel materials Si and GaAs are used and have done a comparative analysis of these devices. For metal contacts and electrodes, aluminum (Al) and Tungsten (W) are used respectively. The device is designed with a constant channel width 10nm and constant height 10nm respectively. Remaining all parameter is common for

both devices. The 3D device structure is designed by python coding and created a TIF3D file. The TIF3D is simulated with Cogenda Visual TCAD [9].

Device simulations and analysis

Above designed devices are simulated with the parameters shown in table 1 using classical drift-diffusion mechanism [9].

$$\nabla\varphi\nabla.\in = -q\,(N_D^{+} + N_A^{-} + p - n) \quad (1)$$

The output characteristics of GAA NW FETs devices have been obtained with varying drain voltage (0-1.0V) on constant gate voltage V_{GS} = 1.0V. The transfer characteristics of GAA NW FET devices have been obtained with varying gate voltage on constant drain voltage V_{DS} = 1.0V. SS (subthreshold swing) is the change in gate voltage per decade and is calculated from transfer characteristics.

$$SS = dV_G / d\log(I_D) \quad (2)$$

From transfer characteristics at constant drain voltage V_D = 0.5V, on current is taken at V_G = 1.0V and off current is taken at V_G = 0.0V. Whereas threshold voltage (V_{TH}) is extracted from active region with constant drain voltage V_D = 0V. At constant drain current (I_D = 6.0E-8) and constant drain voltages (V_{LIN} = 0.05V and V_{SAT} = 1.0V).DIBL is find out from horizontal displacement of I-V characteristics (I_{CD}) for drain voltage V_D=0.05 and 1V [10]

$$I_{CD} = (W_{EFF}/L_G) \times 10^{-7} \quad (3)$$

Whereas W_{EFF} (channel effective length) is defined as:

$$W_{EFF} = 2H_{FIN} + 2W_{FIN,\,eq} \quad (4)$$

Equivalent fin width ($W_{FIN,\,eq}$) [10] is given as,

$$W_{FIN,\,eq} = W_{FIN,\,TOP} + (\beta / \beta+1)\,(W_{FIN,\,BOT} - W_{FIN,\,TOP}) \quad (5)$$

Whereas β,

$$\beta = (2W_{FIN,\,BOT} + W_{FIN,\,TOP}) / (2W_{FIN,\,TOP} + W_{FIN,\,BOT}) \quad (6)$$

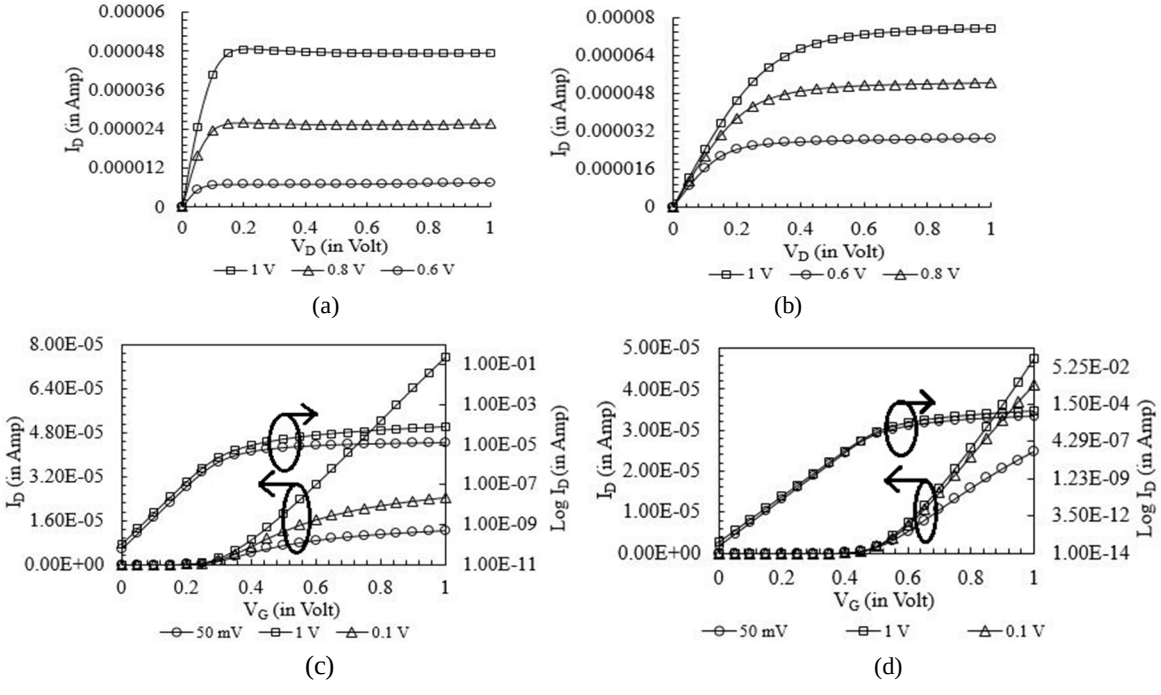

Fig. 2. (a) Output characteristics of GaAs NW FET (at 300^0K) (b) Output characteristics Si NW FET (at 300^0K) (c) Transfer characteristics of GaAs NWT (at 300^0K) (d) Transfer characteristics of Si NWT (at 300^0K)

Figure 2 shows the relation of I_D-V_D and I_D-V_G of devices at 300^0K. Figure 2(a) and 2(c) illustrates that the drain current is directly proportional to the voltage in linear region. It is linearly increasing with drain voltage V_D (V). Further I_D gets saturated w.r.t V_D and it is called saturation region.

Table 2. Extracted Device Parameters of GaAs and Si based NWT within a Temperature Range of 100^0K To 500^0K

Temp. (in K)	DIBL (in mV/V)		SS (in mV/decade)		V_{TH} (in Volt)	
	GaAs NWT	Si NWT	GaAs NWT	Si NWT	GaAs NWT	Si NWT
100K	8.4	30.5	21.5	20.5	0.44	0.295
150K	4.9	12.4	31.3	32	0.43	0.26
200K	3.2	7.4	40.4	42.5	0.425	0.24
250K	2.6	18.5	53	53	0.42	0.2
300K	4	14	62	64	0.405	0.23
350K	6	19.4	72	74	0.38	0.21
400K	10	25.4	84	87	0.36	0.2
450K	13.5	27.68	94	99	0.34	0.165
500K	15.6	32	105	115	0.3	0.15

Table 3. . I_{ON} and I_{ON} / I_{OFF} Ratio of GaAs and Si based NWTs within a Temp Range Of 100^0K To 500^0K

Temp (in K)	I_{ON} (in Amp)		I_{OFF} (in Amp)		I_{ON}/I_{OFF}	
	GaAs NWT	Si NWT	GaAs NWT	Si NWT	GaAs NWT	Si NWT
100K	7.75 E-5	8.58 E-5	7.32 E-18	7.23 E-16	1.05 E+13	1.18 E+11
150K	6.83 E-5	8.28 E-5	1.12 E-17	5.27 E-16	5.69 E+12	1.57 E+11
200K	6.04 E-5	8.00 E-5	3.45 E-16	2.22 E-13	1.75 E+11	3.60 E+8
250K	5.35 E-5	7.76 e-5	2.24 E-15	8.95 E-12	2.21 E+9	8.67 E+6
300K	4.75 E-5	7.55 E-5	5.71 E-14	1.10 E-10	8.14 E+8	6.86 E+5
350K	4.23 E-5	7.34 E-5	5.85 E-13	6.83 E-10	7.31 E+7	1.07 E+5
400K	3.75 E-5	7.14 E-5	3.38 E-12	2.78 E-9	1.15 E+7	2.56 E+4
450K	3.32 E-5	6.94 E-5	1.33 E-11	8.71 E-9	2.60 E+6	7.97 E+3
500K	2.92 E-5	6.73 E-5	4.08 E-11	2.31 E-8	7.51 E+5	2.91 E+3

Further influence of temperature on the performance of the device is investigated. All simulations have been carried out with in temperature of 100^0K to 500^0K and different performance parameters have been extracted. Table II depicts the comparison between SCEs of GaAs and Si based GAA NWTs. Variation of DIBL, SS and V_{TH} with temperature shows the effect of temperature on these devices. SCEs like DIBL, SS, and V_{TH} depends upon the control of gate over the channel.

GaAs NW FETs shows better gate controllability as compared to Si NW FETs, hence smaller value of SS. Minimum SS means high switching speed and hence GaAs NWTs are more suitable for high switching application. It can be observe that below 300^0K for both Si NW FETs and GaAs NW FETs DIBL shows more than one trend whereas above 300^0K it increases with temperature.

On the other side SS will decrease with decrease in temperature and rise with rise in temperature and shown in table II. To obtain better switching characteristics and leakage current reduced to quite a negligible level one needs to increase the threshold voltage level to an acceptable value. Threshold voltage (V_{TH}) will decreases as temperature increases. From table II it is clear that at low temperature value, threshold voltage is more and hence at lower temperature leakage current is very less which will become the possible cause of high I_{ON}/I_{OFF} ratio and hence better switching characteristics.

From table 2 it is clear that GaAs NWT have less SCE as compared to Si NW FETs on the other side GaAs NWTs show higher V_{TH} as compared to Si NWT FETs. Table 3 shows the electrical parameters like I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio of the GaAs and Si based NWTs with in a temp range of 100^0K to 500^0K. At higher temperature both the devices have less I_{ON} current. In case of GaAs GAA NW FETs, the decrease in mobility is more as compared to silicon GAA NW FETs and hence I_{ON} for silicon GAA NW FETs is more as compared to GaAs NW FETs. From table it is clear that Si NWT have high I_{ON} than GaAs NWT at different temperature values.

GaAs NW FETs have higher value of V_{TH} as compared to Si NW FETs due to which GaAs NW FETs have lower value of leakage current as compared to Si NW FETs. From table it is clear that GaAs NW FETs have lower value of leakage current (I_{OFF}) than Si NW FETs at different temperatures. It is also clear that GaAs NW FETs have high I_{ON}/I_{OFF} ratio as compared to Si NW FETs at all temperatures. Hence, GaAs NW FETs show better switching characteristics (I_{ON}/I_{OFF}) as compared to Si NW FETs which means GaAs NW FETs are faster and more suitable for the future CMOS technology than Si NW FETs.

Table 4 shows the comparison between extracted device parameters of GaAs NWT with Si NWTs within a temp range of 100^0K to 500^0K.

Table 4. Comparison between Extracted Device Parameters of GaAs NWT with Si NWTs within a Temp Range of 100^0K To 500^0K

Temp	I_{ON}	I_{ON}/I_{OFF}	SS	DIBL	V_{TH}
100 K	-0.993 times	+0.88E+2 times	+1.048 times	-0.275 times	+1.491 times
150 K	-0.898 times	+0.32E+2 times	-0.978 times	-0.395 times	+1.653 times
200 K	-0.814 times	+0.48E+3 times	-0.95 times	-0.432 times	+1.77 times
250 K	-0.739 times	+2.25E+3 times	Same	-0.140 Times	+2.1 times
300 K	-0.671 times	+1.05E+3 times	-0.968 times	-0.285 times	+1.76 times
350 K	-0.610 times	+5.97E+2 times	-0.972 times	-0.309 times	+1.809 times
400 K	-0.554 times	+3.90E+2 +times	-0.965 times	-0.393 times	+1.8 times
450 K	-0.502 times	+2.83E+2 times	-0.949 times	-0.487 times	+2.60 times
500 K	-0.453 times	+2.22E+2 times	-0.913 times	-0.487 times	+2 times

Conclusion

In this paper, characteristics of gallium arsenide (GaAs) and silicon (Si) based gate all around nanowire FET (GAA NW FET) with triangular cross section area of 20nm gate length were designed and analyzed. From transfer characteristics and output characteristics, performances of above designed devices have been analyzed. GaAs GAA NW FET show better performance in terms of I_{ON} current, switching speed (I_{ON} /I_{OFF}), leakage current, Drain Induced Barrier Lowering (DIBL), Sub-threshold Swing (SS) and threshold voltage (V_{TH} Further Influence of temperature on the performance of device have been studied within temperature range of 100^0K to 500^0K. It was observe that GaAs NW FET can improve the SCEs like low SS and low DIBL. GaAs NW FETs have good gate controllability, it has low leakage current and due to high electron mobility larger current will flow from channel region which leads to high I_{ON} /I_{OFF} ratio. Due to high threshold level (V_{TH}) and high electron mobility, GaAs NW FET have better switching characteristics and hence more suitable for future CMOS technology whereas in the race of high I_{ON} current, Si NW FET will lead.

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